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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/715,081	11/20/2000	Akitaka Nakayama	001542	7823

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EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/715,081	NAKAYAMA ET AL.	
	Examin r	Art Unit	
	Jeffrey A. Shapiro	3653	

-- Th MAILING DATE of this communication appears on th cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/25/03 has been entered.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Kalagnanam et al (US 6,044,361). Kitamura discloses the manufacturing system for printed wiring boards as follows.

As described in Claims 1, 9 and 10;

1. a schedule data storage unit (302) storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;

2. a detecting unit (205) detecting a quantity of printed wiring boards which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of

the printed wiring boards scheduled to be manufactured, according to multiple manufacturing schedule data; (Note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment). Note also figure 11, in which product information (1103), equipment information (1104) and a manufacturing situation (1105) are stored in memory and that network (1108) is connected to processing equipment (1110). See col. 8, lines 36-67. *The system of Kitamura, at the very least, implies that detection is occurring, otherwise, the system would not operate.*)

3. a condition data storage unit (204) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block; (Note that laying out different wiring boards of different types is construed as placing them in a particular area of, for example, a component assembly machine, such that they will be assembled. Note also col. 5, lines 36-55, which indicates that a designer inputs product information and related processing information. See also col. 5, lines 31-35. Note also col. 1, lines 7-16, which indicates that this designing concerns a semiconductor device and a process procedure. Such a device could be construed as requiring several printed wiring boards and the associated design data input by the designer can be

construed to be information on where the machine will place various electronic components on said board. Even if this is not the case, it appears that it would be an obvious substitution to adapt such a computer based manufacturing system to integrate a printed circuit wiring board design operation with an associated assembly or fabrication process.)

4. a dividing unit dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data; (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that such a system as described by Kitamura would necessarily be expected to group particular product based on a wide variety of criteria, including the particular process required, the particular model of board, as well as the manufacturing load on a particular piece of equipment. See col. 9, lines 22-27, for example.)

5. a determining unit determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that a determining unit can be construed to be a number of

components of the system of Kitamura. For example, as described above, the system identifies the condition of a particular piece of equipment as well as how many items individually or in lots are being produced at which piece of equiment. The system of Kitamura necessarily must detect information about the manufacturing process through a particular means, otherwise, it would not work. See also col. 5, lines 12-27, as well as figures 11-13. Note element 1304 in figure 13, which "verifies the process procedure".)

As described in Claim 2;

6. said detecting unit, if a manufacturing quantity of the boards of a certain kind cannot be divided completely by a maximum number of the boards which can be laid out in a single predetermined manufacturing block, detects printed wiring boards corresponding to a number smaller than said maximum number or an excess of boards of said fraction. (Again, note that such a system as that of Kitamura necessarily maximizes the most product that can fit on a particular machine so as to efficiently process the required product as determined by customer orders. As described above, the system of Kitamura necessarily describes load balancing of various production machines, and would not work otherwise in such an environment.)

As described in Claim 3;

7. the manufacturing condition data is data produced by combining orders with product data (note that customer orders and product data are necessarily combined in order to move material through the system—see also manufacturing situation memory (1105) and product information memory (1103), which are both used to optimize work flow through the production line);

As described in Claim 4;

8. the order data includes a shipment date (note that it is inherent and obvious that product moving through the system would have a shipment date assigned to it);

As described in Claims 5 and 6;

9. the product data includes the number of layers of the printed wiring boards (note that it would be obvious to include the number of layers as design and processing parameters since the process of Kitamura is for semiconductor manufacturing—see abstract, lines 1 and 2);

Kitamura does not expressly disclose handling fractional printed circuit boards or fractional groups of printed circuit boards.

Kalagnanam et al discloses handling fractional items in a manufacturing system with inventory matching. See col. 1, lines 48-67, col. 2, lines 1-67, col. 3, lines 1-67, col. 4, lines 1-67, and col. 5, lines 1-41.

Both Kitamura and Kalagnanam et al are analgous art because they both concern manufacturing inventory and scheduling.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the optimization routines of Kalagnanam et al in the system of Kitamura to identify and match partial items, such as printed circuit boards or partial lots/groups of printed circuit boards with orders or other requirements.

The suggestion/motivation would have been to reduce waste of PC-Boards. See Kalagnanam et al, col. 2, lines 33-37.

Therefore, it would have been obvious to combine Kitamura and Shin et al in order to obtain the invention as specified in Claims 7 and 8.

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Kalagnanam et al and further in view of Shin et al. Kitamura discloses the system as described above. Kitamura does not expressly disclose, but Shin et al discloses the following.

As described in Claim 7;

10. a CAD data creating unit (see col. 17, lines 21-23) creating CAD data corresponding to a combination determined by said determining unit;

11. a CAD data converting unit creating CAM data or CAT data corresponding to CAD data created by said CAD data creating unit (see col. 17, lines 21-47);

As described in Claim 8;

12. a manufacturing unit group (20, 22, 24, 26 and 28) carrying out a manufacturing process for the printed wiring board using the CAM data or the CAT data created by said CAD data creating unit;

Both Kitamura and Shin et al are analgous art because they both concern manufacturing pc-boards.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the CAD and CAT creating units and converting units to create product and test data, as described by Shin et al, for use by the system of Kitamura.

The suggestion/motivation would have been to provide direct input of product information required for production and testing of PC-Boards.

Therefore, it would have been obvious to combine Kitamura and Shin et al in order to obtain the invention as specified in Claims 7 and 8.

Response to Arguments

5. Applicant's arguments filed 12/10/02 have been fully considered but they are not persuasive. See discussion above. Applicant's representative is encouraged to contact

the Examiner at the phone contact below, should clarification or consultation be required.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (703)308-3423. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald P. Walsh can be reached on (703)306-4173. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-1113.

Jeffrey A. Shapiro
Examiner
Art Unit 3653

October 19, 2003

DONALD P. WALSH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600